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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,132	10/16/2001	Alessandro Zafarana	856063.715	9379

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SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,132	ZAFARANA ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 13-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 13-25* is/are rejected.

7)☒ Claim(s) *3-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 6-12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on March 28, 2005.

Claim Objections

2. Claim 2 is objected to because of the following informalities: on line 6, "said second supply voltage reference" is interpreted as "and said second supply voltage reference". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 2 has the limitation "said controller ... supplies an internal control voltage directly to said equivalent droop resistor" (line 13), whereas the specification states "controller 4 ... outputs an internal control current directly to the equivalent droop resistor" (paragraph 50).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 and 2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: whether "being connected to said common bus" modifies the error amplifier or the equivalent droop resistor; and whether "receiving an output current signal (Iout) from said plurality of VRMs" modifies the error amplifier or the equivalent droop resistor.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: whether "arranged to output a control voltage signal to said plurality of VRMs" modifies the first summing node or the error amplifier.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Chesavage, U.S. Patent No. 5,834,925.

As per claim 1, Chesavage teaches a managing system for managing a plurality of VRMs associated with a plurality of microprocessors and connected in parallel together between first and second voltage references, said VRMs having output terminals connected together and arranged to communicate over a common bus, wherein said managing system comprises:

an error amplifier being input an output voltage signal from said plurality of VRMs (fig. 4, error amplifier 50 receives feedback voltage via resistor 53a), a reference voltage (fig. 4, Vref), and a droop voltage produced through an equivalent droop resistor receiving an output current signal (Iout) from said plurality of VRMs (fig. 4, voltage across resistor 56a which receives output from current amplifier 55a) and being connected to said common bus (fig. 4, error amplifier 50a connected to common voltage bus via feedback loop), said error amplifier effecting a comparison of said input signals to generate a control voltage signal to said plurality of VRMs (fig. 4, error amplifier 50a sends control signal to PWM 54a); and

a controller connected to said equivalent droop resistor (fig. 4, current amplifier 55a, current amplifier 59, or resistor 57a).

6. Claims 13-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Small, U.S. Patent No. 4,717,833.

As per claim 13, Small discloses a control system for controlling a first voltage reference module that outputs an output voltage, comprising:

a first error amplifier having a first input and an output, the first input being coupled to the output (fig. 1, amplifier 22 having a first input coupled to output via R8);

a feedback resistor coupled between the output voltage and the first input of the first error amplifier (fig. 1 resistor R7 coupled between Vout and first input);

a first current generator coupled to the first input of the first error amplifier (fig. 1, resistor R8); and

a controller having second current generator coupled to the first input of the error amplifier (fig. 1, resistor R4 coupled to input of amplifier 22), the second current generator being responsive to a voltage on a common bus connected between the first voltage reference module and a second voltage reference module (fig. 1, current at node 14 is responsive to voltage of parallel bus at node 15; fig. 4, parallel bus at node 69 is connected between power supplies 62-1 to 62-N; col. 3, lines 31-44; col. 6, lines 6-16).

As per claim 14, Small discloses the first error amplifier further comprises a second input coupled to a voltage reference (fig. 1, Vref coupled to other input of amplifier 22).

As per claim 15, Small discloses a second error amplifier having a first input coupled to the common bus, a second input coupled to one of the inputs of the first error amplifier, and an output coupled to the second current generator (fig. 1, amplifier 11 with input 2 coupled to parallel bus via resistor R2, input 3 coupled to input of amplifier 22 via resistor R5, and output 1 coupled to resistor R4).

As per claim 16, Small discloses a second error amplifier having a first input coupled to the common bus, a second input coupled to the first input of the first error amplifier, and an output coupled to the second current generator (fig. 1, amplifier 11 with input 3 coupled to parallel bus via resistor R1, input 2 coupled to first input of amplifier 22 via resistor R3 and capacitor C2, and output 1 coupled to resistor R4).

As per claim 17, Small discloses a share resistor coupled between the common bus and the second input of the second error amplifier (fig. 1, resistor R2).

As per claim 18, Small discloses a first resistor connected between the share resistor and the first input of the second error amplifier (fig. 1, resistor R2; fig. 3, resistance of element 36 between R3 and input 3 of parallel amplifier); and a second resistor connected between the share resistor and the second input of the second error amplifier (fig. 3, resistor R7 between R3 and input 2).

As per claim 25, Small discloses the output and first input of the first error amplifier are feedback-connected to one another (fig. 1, via resistor R8).

As per claim 19, Small discloses a control system for controlling a first voltage reference module that outputs an output voltage, comprising:

a first error amplifier having first and second inputs and an output (fig. 1, amplifier 22);

a feedback resistor coupled between the output voltage and the first input of the first error amplifier (fig. 1, resistor R7 coupled between Vout and first input); and

a second error amplifier having a first input coupled to a common bus (fig. 1, amplifier 11 has input 2 coupled to parallel bus at node 15), a second input coupled to one of the inputs of the first error amplifier (fig. 1, input 3 coupled to input of amplifier 22 via resistor R5), and an output coupled to the first input of the first error amplifier (fig. 1, output 1 coupled amplifier 22 via resistor R4), the common bus being connected to the first voltage reference module and a second voltage reference module (fig. 4, parallel bus at node 69 connected to power supplies PS 62-1 to 62-N; col. 3, lines 31-44; col. 6, lines 6-16).

As per claim 20, Small discloses a first current generator coupled between the output of the second error amplifier and the first input of the first error amplifier (fig. 1, resistor R4; fig. 5, voltage to current generator between error amplifier and parallel amplifier).

As per claim 21, Small discloses a second current generator coupled to the first input of the first error amplifier (fig. 1, resistor R8).

As per claim 22, Small discloses the first error amplifier further comprises a second input coupled to a voltage reference (fig. 1, Vref coupled to other input of amplifier 22).

As per claim 23, Small discloses a share resistor coupled between the common bus and the second input of the second error amplifier (fig. 1, resistor R1).

As per claim 24, Small discloses a first resistor connected between the share resistor and the first input of the second error amplifier (fig. 3, resistor R7 between R3 and input 2 of parallel amplifier); and a second resistor connected between the share resistor and the second input of the second error amplifier (fig. 1, resistor R1; fig. 3, resistance of element 36 between resistor R3 and input 3 of parallel amplifier).

Allowable Subject Matter

7. Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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April 19, 2005

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100